WHAT IS CLAIMED IS:

1. A semiconductor circuit having a storage unit storing a first multi-bit data and a comparator comparing said first data with a second multi-bit data, wherein

an active state of said comparator is controlled based on a first control signal for controlling the output of said first data from said storage unit.

2. The semiconductor circuit according to claim 1 wherein

said storage unit includes a sense amplifier outputting a first activation signal,

an active state of said sense amplifier is controlled by said first control signal, and

said comparator is controlled based on said first activation signal outputted from said sense amplifier.

3. The semiconductor circuit according to claim 2 wherein said comparator includes:

a plurality of exclusive OR circuits performing an exclusive OR operation of the corresponding bits between said first data and said second data; and

an AND circuit performing an AND operation of exclusive OR signals outputted from said plurality of exclusive OR circuits, respectively.

4. The semiconductor circuit according to claim 3 wherein

active state/inactive state of said exclusive OR circuits are controlled by said first activation signal.

5. The semiconductor circuit according to claim 4 wherein

said AND circuit is a dynamic circuit which performs during its active state an AND operation of exclusive OR signals outputted from said plurality of exclusive OR circuits, and to which precharging is executed during its inactive state, active state/inactive state of said AND circuit being controlled by a clock signal.

6. The semiconductor circuit according to claim 3 further including:

a delay circuit that converts said first activation signal to a second activation signal by giving said first activation signal a time delay equal to or more than the operation time on said exclusive OR circuit, wherein

said AND circuit is a dynamic circuit which performs during its active state an AND operation of exclusive OR signals outputted from said plurality of exclusive OR circuits, and to which precharging is executed during its inactive state, active state/inactive state of said AND circuit being controlled by said second activation signal.

7. The semiconductor circuit according to claim 4 further including:

a delay circuit that converts said first activation signal to a second activation signal by giving said first activation signal a time delay equal to or more than the operation time on said exclusive OR circuit, wherein

said AND circuit is a dynamic circuit which performs during its active state an AND operation of exclusive OR signals outputted from said plurality of exclusive OR circuits, and to which precharging is executed during its inactive state, active state/inactive state of said AND circuit being controlled by said second activation signal.

8. The semiconductor circuit according to claim 6 wherein

said AND circuit includes:

a group of transistors performing operation that are connected in parallel to each other;

a transistor of a first conductivity type connecting respective one ends of said transistor group to a fixed power source; and

a transistor of a second conductivity type connecting respective the other ends of said transistor group to ground, and

said second activation signal is used to control such that only one of said transistor of the first conductivity type and said transistor of the second conductivity type enters the on state.

9. The semiconductor circuit according to claim 7 wherein

said AND circuit includes:

a group of transistors performing operation that are connected in parallel to each other;

a transistor of a first conductivity type connecting respective one ends of said transistor group to a fixed power source; and

a transistor of a second conductivity type connecting respective the other ends of said transistor group to ground, and

said second activation signal is used to control such that only one of said transistor of the first conductivity type and said transistor of the second conductivity type enters the on state.

10. The semiconductor circuit according to claim 1 wherein

said comparator does not perform any comparison processing when said first

data is written in said storage unit, and performs a comparison processing when said first data is read from said storage unit.

11. The semiconductor circuit according to claim 10 wherein

said storage unit further includes a logic gate for controlling the output of said first control signal, said logic gate being controlled by a second control signal.

12. The semiconductor circuit according to claim 6 wherein

an output signal from said AND circuit maintains a predetermined initialization state until a desired output signal outputted from said exclusive OR circuit is established.

13. The semiconductor circuit according to claim 7 wherein

an output signal from said AND circuit maintains a predetermined initialization state until a desired output signal outputted from said exclusive OR circuit is established.

14. The semiconductor circuit according to claim 12 wherein

said AND circuit includes a transistor for initialization, one end of which is connected to the output side of said AND circuit, and the other end is connected to a fixed power source, and

said transistor for initialization is controlled based on said second activation signal so as to become conductive until a desired output signal outputted from said exclusive OR circuit is established.

15. The semiconductor circuit according to claim 13 wherein

said AND circuit includes a transistor for initialization, one end of which is

connected to the output side of said AND circuit, and the other end is connected to a fixed power source, and

said transistor for initialization is controlled based on said second activation signal so as to become conductive until a desired output signal outputted from said exclusive OR circuit is established.

16. The semiconductor circuit according to claim 14 further including:

a pulse generator generating a pulse signal in synchronization with a clock signal; and

a latch circuit having a Reset input part to which said pulse signal is inputted, a Set input part to which said second activation signal is inputted, and an output part outputting a third activation signal generated from said pulse signal and said second activation signal, wherein

said transistor for initialization is controlled by said third activation signal.

17. The semiconductor circuit according to claim 15 further including:

a pulse generator generating a pulse signal in synchronization with a clock signal; and

a latch circuit having a Reset input part to which said pulse signal is inputted, a Set input part to which said second activation signal is inputted, and an output part outputting a third activation signal generated from said pulse signal and said second activation signal, wherein

said transistor for initialization is controlled by said third activation signal.

18. The semiconductor circuit according to claim 16 wherein

active state/inactive state of said AND circuit are controlled by said third activation signal.

19. The semiconductor circuit according to claim 17 wherein

active state/inactive state of said AND circuit are controlled by said third activation signal.

20. The semiconductor circuit according to claim 1 wherein

said comparator includes:

a plurality of exclusive OR circuits performing an exclusive OR operation of the corresponding bits between said first data and said second data; and

said AND circuit is a dynamic circuit which performs during its active state an AND operation of exclusive OR signals outputted from said plurality of exclusive OR circuits, and to which precharging is executed during its inactive state, active state/inactive state of said AND circuit being controlled by said first control signal.

21. The semiconductor circuit according to claim 20 wherein

said AND circuit includes a group of transistors performing an AND operation, and

said exclusive OR circuit is a circuit outputting a signal not activating said group of transistors of said AND circuit until said first data is inputted.

22. The semiconductor circuit according to claim 20 wherein

said first data and a third data having a complementary relationship with said first data are inputted to said exclusive OR circuit.

23. The semiconductor circuit according to claim 22 wherein

the output of said first data and said third data is controlled by said first control signal.